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EXAMINER	
LAI, VINCENT	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,025	SHIPPY, DAVID	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 16-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 16-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
10/29/2006

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 have been considered by the examiner.

Response to Amendment

2. Acknowledgment is made of the amendment to claims and title.

3. Objections to the title are withdrawn after considering amendments.

4. 35 U.S.C. 101 rejections are withdrawn since claims 10-12 (among others) have been cancelled.

Response to Arguments

5. Applicant's arguments filed 4 August 2006 have been fully considered but they are not persuasive.

Applicant argues, "Sollars does not teach or suggest that each register file of the plurality of register files at least corresponds to at least one thread of the plurality of threads, as recited in claim 1...Rather, Sollars teaches that sets of control register correspond to a privilege level."

Cited in the action is column 2, lines 2-6, which says, "At the third highest level of the logical hierarchy is a number of control register sets for controlling concurrent execution of multiple peer process threads (hereinafter simply threads) for each of the concurrently executing peer contexts." There is a mention of hierarchy, but hierarchy is simply the manner in which the register files are organized. Sollar goes on to say, "in one implementation of the preferred embodiment, eight sets of context control registers are provided for concurrently supporting up to eight active contexts, and 64 sets of thread control registers are provided for concurrently supporting up to eight active threads for each of the active contexts" (Column 2, lines 7-12). Thus control registers do indeed correspond to threads and not merely a privilege level. Given this, the register file that contains the control registers must indeed also correspond to a thread.

Applicant argues, "Sollars does not teach or suggest a plurality of control bit sets that are configured to allow a thread associated status and control register to utilize other register files associated with other threads." The Applicant goes on to admit that Sollar "teaches that threads may be allowed to access and modify a peer thread's control register sets. However, the Office Action alleges that the primary and secondary operand register files are equivalent to the plurality of register files of claim 1. Thus, the Office Action has not shown that Sollars teaches of fairly suggests a plurality of control bit sets that are configured to allow a thread to utilize other operand register files associated with other threads."

Sollars goes on to discuss the conditions in which threads may be allowed to access and modify a peer thread's control register sets (See column 16, lines 5-15). In the discussion, Sollars mentions that certain execution exceptions may necessitate such actions to be taken. These exceptions are stored within the register file (See figure 9E and column 13, lines 25-28: the SWFLAG register contains control bits for traps) and thus there are indeed a plurality of control bit sets that are configured to allow a thread to utilize other operand register files associated with other threads.

Applicant argues, "the Office Action [offers] no analysis as to why the [cited lines are] somehow equivalent to separately enabling a thread to read from a register file associated with a different thread or separately enabling a thread to write to a register file associated with a different thread."

Please refer to arguments presented above. The TCTCL is in control of the various control registers, including the SWFLAG, which does allow for access other register files, as explained above.

All arguments related to the new claims are addressed below in the rejections.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-5, 7-8 rejected under 35 U.S.C. 102(b) as being anticipated by Sollars (US Pat. No. 5,900,025).

Regarding **independent claim 1**, Sollars discloses *an architected register file system at least configured to utilize a plurality of threads, comprising: a plurality of register files* [see Sollars, Col. 5, lines 21-30], *wherein each register file of the plurality of register files at least corresponds to a respective thread of the plurality of threads* [see Sollars, Col. 5, lines 24-30; Examiner's note: In this cite, Sollars discloses a multi-dimensional register file which would allow for multiple threads to occupy a register file in a subset dimension. This idea is illustrated in Fig. 2a of US Pat. No. 6,081,880 (to Sollars as well) incorporated by reference by Sollars in '025]*; a plurality of Status and Control Registers (SCR)* [see Sollars, Fig. 1, element 20a; Col. 5, lines 31-34], *wherein each SCR corresponds to a respective thread of the plurality of threads* [see Sollars, Col. 2, lines 2-6]*; and a plurality of control bit sets, wherein each control bit set corresponds to at least one SCR* [see Sollars, Fig. 5; Examiner's note: Fig. 5 illustrates an SCR containing control bit sets.], *and wherein each control bit set is at least configured to allow a thread associated with an associated SCR to utilize other register files associated with other threads* [see Sollars, Col. 15, lines 60-66].

Regarding **claim 2**, Sollars discloses *the architected register file system of claim 1, wherein the architected register file system further comprises a decoder, wherein the decoder at least determines desired operations for an instruction* [see Sollars, Col. 2, line 64 to Col. 3, line 1; Examiner's note: It is inherent that the function of a decoder is to determine the operations requested of an instruction.].

Regarding **claim 3**, Sollars discloses *the architected register file system of claim 1, wherein plurality of control bits further comprise a plurality of bit doublets* [see Sollars, Fig. 9A, elements "sl" and "ll"], *wherein a first bit of a bit doublet corresponds to a read function* [see Sollars, Col. 10, lines 57-62, "...of a load operation is to be locked..."], *and wherein a second bit of the bit doublet corresponds to a write function* [see Sollars, Col. 10, lines 51-57, "...of a store operation is to be locked..."].

Regarding **claim 4**, Sollars discloses *the architected register file system of claim 3, wherein the architected register file system further comprises: an address control, wherein the address control at least determines addresses with the plurality of register files* [see Sollars, Col. 5, lines 24-30; Examiner's note: Sollars incorporates US Pat. No. 6,081,880 (to Sollars), which discloses the operation of the operand, register file (Sollars ('025), Fig. 2, element 22a). In Figure 2a of '880, Sollars shows a multidimensional register file wherein element 22' is used to address register files 22a-*. Therefore, by reference, Sollars shows an address control that determines the address of a plurality of register files.]*; and at least one execution unit* [see Sollars, Fig. 2,

element 14], *wherein the execution is at least configured to perform the operations of a input instruction within the plurality of register files* [see Sollars, Col. 6, lines 24-34].

Regarding **claim 5**, Sollars discloses *the architected register file system of claim 3, wherein the plurality of bit doublets further comprises that each bit doublet at least corresponds to enabling the use of at least one register file associated with another thread* [see Sollars, Col. 10, lines 51-62 (enabling writing and reading to/from a register file); Col. 15, lines 60-66 (accessing other multiple threads)].

Regarding **independent claim 7**, Sollars discloses *a method for utilizing a plurality of register files* [see Sollars, Col. 5, lines 21-30] *with associated SCRs in a multithread system* [see Sollars, Fig. 1, element 20a; Col. 5, lines 31-34], *wherein each register file is at least associated with one thread of a plurality of threads* [see Sollars, Col. 5, lines 24-30; Examiner's note: In this cite, Sollars discloses a multi-dimensional register file which would allow for multiple threads to occupy a register file in a subset dimension. This idea is illustrated in Fig. 2a of US Pat. No. 6,081,880 (to Sollars as well) incorporated by reference by Sollars in '025], *comprising: receiving an instruction for a first thread of the plurality of threads* [see Sollars, Col. 2, line 64 to Col. 3, line 1, "...fetching...instructions for the active threads..."], *wherein the first thread is at least associated with a first SCR* [see Sollars, Col. 2, lines 2-6; Examiner's note: Since the SCR is associated with a threads register file, it is inherently associated with the thread.]; *decoding the instruction to at least determine performance operations* [see

Sollars, Col. 2, line 64 to Col. 3, line 1, "...decoding...instructions for the active threads..."]; *determining if the first thread is enabled to at least utilize register files associated with other threads* [see Sollars, Col. 10, lines 57-62]; *and executing the instruction, wherein the step of executing utilizes at least one register file associated with a second thread of the plurality of threads* [see Sollars, Col. 15, lines 60-66].

Regarding **claim 8**, Sollars discloses *the method of claim 7, wherein the step of determining if the first thread is enabled, further comprises measuring logical levels of control bits associated with the first SCR, wherein the control bits comprise a plurality of bit doublets* [see Sollars, Fig. 9A, elements "sl" and "ll"], *and wherein each bit doubled at least corresponds to enabling the use of at least one register file associated with another thread* [see Sollars, Col. 10, lines 51-62; Col. 15, lines 60-66].

Claims 10-15 have been cancelled.

Regarding **claim 16**, Sollars discloses a method for utilizing a plurality of register files in a multithread system, the method comprising:

receiving an instruction for a first thread having an operations code field, a write field, and one or more read fields, wherein the operations code field defines a desired operation for the instruction, wherein the write field defines an address location to which a result of the operation is to be stored, and wherein the at least one read field defines

an address location from which data is to be read for the operation (See figure 16A: Generic instruction format);

decoding the instruction (See column 6, lines 16-18: The IFU decodes instructions);

setting a first status and control register associated with the first thread and a second status and control register associated with a second thread based on the decoding of the instruction (Instructions are meant to set status and configure registers accordingly), wherein a first register file is associated with the first thread and a second register file is associated with the second thread; determining whether the first thread is permitted to utilize the second register file associated with the second thread based on at least one of the first status and control register or the second status and control register (See column 16, lines 5-15); and if the first thread is permitted to utilize the second register file, performing the operation utilizing the second register file by writing to or reading from the second register file associated with the second thread (See column 13, lines 25-38: Once an exception is executed upon being encountered).

Regarding **claim 17**, Sollars discloses the method of claim 16, wherein performing the operation comprises: reading data from the second register file based on an address in a read field within the one or more read fields (See column 15, lines 60-66).

Regarding **claim 18**, Sollars discloses the method of claim 16, wherein performing the operation comprises: writing a result of the operation to the second register file based on an address in the write field (See figure 16A: Writing is done according to the instruction).

Claims 19-21 are rejected for reasons similar to claims 16-18.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sollars.

Regarding **claim 6**, Sollars discloses the limitations as stated in **claim 5**.

Sollars also discloses *one bit* [of a doublet] *is at least configured to correspond to a read function* [see Sollars, Col. 10, lines 57-62, "...of a load operation is to be locked..."] and *one bit* [of a doublet] *is at least configure to correspond to a write function* [see Sollars, Col. 10, lines 51-57, "...of a store operation is to be locked..."].

Sollars does not explicitly disclose *a logic high or '1'* enabling *the first thread to read from another register file* or *a logic high or '1'* enabling *the first thread to write to another register file*.

However, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a logic high value to correspond to the enablement of a value stored within a register. At the time of invention, the use of a logic high signal as an indication of an enabled function would have been common knowledge, such as the concept of register flags indicating certain conditions. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize an active-high scheme to enable access to a register file.

Regarding **claim 9**, Sollars discloses the limitations as stated in **claim 8**.

Sollars does not explicitly disclose *determining if any bits are `1` or logic high, wherein the `1` or the logic high enables the first thread to read or write to another register file.*

However, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a logic high value to correspond to the enablement of a value stored within a register. At the time of invention, the use of a logic high signal as an indication of an enabled function would have been common knowledge, such as the concept of register flags indicating certain conditions. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize an active-high scheme to enable access to a register file.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vincent Lai
Examiner
Art Unit 2181

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October 26, 2006

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10/26/2006